AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-15 (Canceled).

16. (new) A nonvolatile memory comprising:

a plurality of nonvolatile memory cells; and

an error correcting circuit,

wherein a program command accompanied with address information and first data are received from outside,

wherein, in a program operation executed in response to said program command, first nonvolatile memory cells of said plurality of nonvolatile memory cells are selected in accordance with said address information and programmed with said first data,

wherein, after said first nonvolatile memory cells are programmed with said first data in said program operation, second nonvolatile memory cells of said plurality of nonvolatile memory cells are selected and second data stored therein are read out,

wherein said error correcting circuit judges whether said second data includes one or more errors and corrects said

second data to create third data when said second data includes one or more errors, and

wherein said second nonvolatile memory cells are programmed with said third data after said second data is corrected by said error correcting circuit.

17. (new) A nonvolatile memory according to Claim 16, wherein, after said first data is programmed and before said second nonvolatile memory cells are selected:

said first nonvolatile memory cells are selected and fourth data stored therein is read out,

said error correcting circuit judges whether said fourth data includes errors which are correctable or not correctable,

said first nonvolatile memory cells are programmed again with said first data if said fourth data includes errors which are not correctable by said error correcting circuit, and

programming of said first nonvolatile memory cells with said first data is completed if said fourth data includes errors which are correctable by said error correcting circuit.

18. (new) A nonvolatile memory according to Claim 17, wherein, after said first data is programmed:

said error correcting circuit judges whether said fourth data includes errors which are correctable or not correctable, and

when said error correcting circuit judges that said fourth data includes errors which are not correctable, third nonvolatile memory cells of said plurality of nonvolatile memory cells, different from said first nonvolatile memory cells, are selected and programmed with said first data.

19. (new) A nonvolatile memory according to Claim 18, further comprising a controller including said error correcting circuit.

20. (new) A nonvolatile memory according to Claim 19, wherein:

said controller further includes a buffer memory, and

said first data is stored in said buffer memory until completion of programming with said first data.

21. (new) A nonvolatile memory according to Claim 16, wherein each of said plurality of nonvolatile memory cells is a one-bit memory cell.

22. (new) A nonvolatile memory according to Claim 16, wherein each of said plurality of nonvolatile memory cells is a multiple-bit memory cell.